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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,498	08/24/2001	Vivek Subramanian	10519/30	3758

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EXAMINER	
VU, DAVID	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 06/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/939,498	SUBRAMANIAN ET AL.	
	Examiner	Art Unit	
	DAVID VU	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *95-125* is/are pending in the application.

4a) Of the above claim(s) *101-106* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *95-100 and 107-125* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4,7,10-1* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless-
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty inthe English language; or
>
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

1. Claims 95 and 97-100 are rejected under 35 U.S.C. 102(e) as being anticipated by Hart et al., (US 5,970,372).

Hart et al., in related text (Col. 9, Lines 49-62; Col. 7, Lines 3-15 and Col. 13, Line. 41-Col. 14, Line. 30) and figure (Fig. 2) disclose a process for fabricating a state change element in a 3-D semiconductor memory device comprising the steps of: forming a semiconductor layer 201; oxidizing at least a portion of the semiconductor layer in a plasma to form an oxide antifuse layer 202 overlying the semiconductor layer 201. The above process was repeating for multiple memory layers, each memory layer comprising vertically fabricated memory cells (See Col. 9, Line 63-Col. 12, Line 32 and Figures. 7-10B).

2. Claims 116-119 are rejected under 35 U.S.C. 102(e) as being anticipated by Hart et al., (US 5,970,372).

In re claims 116-118, Hart et al., in related text (Col. 9, Lines 49-62; Col. 7, Lines 3-15 and Col. 13, Line. 41-Col. 14, Line. 30) and figure (Fig. 2) disclose a process for fabricating a single element antifuse in a 3-D semiconductor memory device comprising: forming a first active electrode layer 201; oxidizing at least a portion of the first active electrode layer in a plasma to form an oxide antifuse layer 202 thereon; and forming a second active electrode layer 203 overlying and in intimate contact with oxide antifuse layer 202.

In re claim 119, the process further comprising forming a first conductor lead below the first active electrode layer and forming a second conductor lead above the second active electrode layer, wherein each of the first and second conductor leads are orthogonally disposed relative to one another (See Col. 9, Line 63-Col. 12, Line 32 and Figures. 7-10B).

3. Claims 120-121 are rejected under 35 U.S.C. 102(e) as being anticipated by Hart et al., (US 5,970,372).

In re claim 120, Hart et al., in related text (Col. 9, Lines 49-62; Col. 7, Lines 3-15 and Col. 13, Line. 41-Col. 14, Line. 30) and figure (Fig. 2) disclose a process for fabricating a 3-D semiconductor memory device comprising the steps of: forming a first stack comprising a state change element 202; and forming a second stack comprising a state change element overlying the first stack (See Col. 9, Line 63-Col. 12, Line 32 and Figures. 7-10B), wherein forming each of the first stack and the second stack comprises forming a semiconductor layer 201; and

oxidizing at least a portion of the semiconductor layer in a plasma to form an oxide antifuse layer 202 overlying the semiconductor layer 201.

In re claim 121, the process further comprising forming orthogonally disposed conductor leads above and below each of the first and second stacks (See Col. 9, Line 63-Col. 12, Line 32 and Figures. 7-10B).

4. Claim 125 is rejected under 35 U.S.C. 102(e) as being anticipated by Hart et al., (US 5,970,372).

Hart et al., in related text (Col. 9, Lines 49-62; Col. 7, Lines 3-15 and Col. 13, Line. 41-Col. 14, Line. 30) and figure (Fig. 2) disclose a process for fabricating a pillar in a 3-D semiconductor memory device, wherein the pillar includes a steering element 201 and a state change element 202 vertically arranged between orthogonally disposed conductors leads (See Col. 9, Line 63-Col. 12, Line 32 and Figures. 7-10B), the process comprising the steps of: forming a semiconductor layer 201; and oxidizing at least a portion of the semiconductor layer 201 in a plasma to form an oxide antifuse layer 202 overlying the semiconductor layer 201.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 107, 109-115 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Hart et al., (US 5,970,372) in view of McCollum et al.,(US 5,763,299).

Hart et al., in related text (Col. 9, Lines 49-62; Col. 7, Lines 3-15 and Col. 13, Line. 41-Col. 14, Line. 30) and figure (Fig. 2) disclose a process for fabricating a multiplayer amorphous silicon antifuse device comprising: forming a first conductor layer 102; forming a first semiconductor layer 201 overlying the conductor layer 102; oxidizing at least a portion of the first semiconductor layer in a plasma to form an oxide layer 202 thereon; forming a second semiconductor layer 203 overlying the oxide layer 202. The above process was repeating for multiple memory layers, each memory layer comprising vertically fabricated memory cells (See Col. 9, Line 63-Col. 12, Line 32 and Figures. 7-10B).

Hart et al. fails to expressly disclose sequentially etching the second semiconductor layer, the oxide layer, the first semiconductor layer and the first conductor layer to form a line;

McCollum et al., in related text (Col. 6, Lines 43-50) and figures (Fig. 3b) disclose an etching step after completion of the stacked antifuse structure 24.

However, given the substantial Hart et al., in view of McCollum et al., it would have been obvious to one with ordinary skill in the art at the time of the invention using a single etch step for forming the stacked antifuse structure. An advantage of a McCollum et al. invention is that the number of mask, deposition, or etching steps is reduced.

6. Claims 122 and 124 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Hart et al., (US 5,970,372) in view of McCollum et al.,(US 5,763,299).

Hart et al., in related text (Col. 9, Lines 49-62; Col. 7, Lines 3-15 and Col. 13, Line. 41-Col. 14, Line. 30) and figure (Fig. 2) disclose a process for fabricating a line comprising: forming a first conductor layer 102; forming a first semiconductor layer 201 overlying the conductor layer 102; oxidizing at least a portion of the first semiconductor layer in a plasma to form an oxide layer 202 thereon; forming a second semiconductor layer 203 overlying the oxide layer 202; etching the second semiconductor layer, the oxide layer, the first semiconductor layer and the first conductor layer to form a line. The above process was repeating for multiple memory levels, in which a first conductor layer of the first line orthogonal to the first conductor layer of the second line (See Col. 9, Line 63-Col. 12, Line 32 and Figures. 7-10B).

Hart et al. fails to expressly disclose sequentially etching the second semiconductor layer, the oxide layer, the first semiconductor layer and the first conductor layer to form a line;

McCollum et al., in related text (Col. 6, Lines 43-50) and figures (Fig. 3b) disclose an etching step after completion of the stacked antifuse structure 24 by using the oxide plasma process.

However, given the substantial Hart et al., in view of McCollum et al., it would have been obvious to one with ordinary skill in the art at the time of the invention using a single etch step for forming the stacked antifuse structure. An advantage of a McCollum et al. invention is that the number of mask, deposition, or etching steps is reduced.

7. Claim 123 is rejected under 35 U.S.C. 102(e) as being anticipated by Hart et al., (US 5,970,372).

In re claim123, Hart et al., in related text (Col. 9, Lines 49-62; Col. 7, Lines 3-15 and Col. 13, Line. 41-Col. 14, Line. 30) and figure (Fig. 2) disclose a process for fabricating a 3-D semiconductor memory device comprising the steps of: forming a first stack comprising a steering element 201 and a state change element 202. The above process was repeating for multiple memory levels (See Col. 9, Line 63-Col. 12, Line 32 and Figures. 7-10B).

Hart et al. fails to expressly disclose etching the stack to form a line by using a plasma oxidation process.

McCollum et al., in related text (Col. 6, Lines 43-50) and figures (Fig. 3b) disclose an etching step after completion of the stacked antifuse structure 24 by using the oxide plasma process. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the method of McCollum et al. in the process of Hart et al., within the general skill of a worker in the art, to select a known method on the basis of its suitability for its intended use is a matter of obvious design choice.

8. Claim 96 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hart et al.,(US 5,970,372) in view of Miyasaka (US 6,444,507).

Hart et al., disclose all claimed subject matter, but fails to expressly disclose the temperature of the oxidation process.

Miyasaka et al, in related text, (Col. 25, Line 63-Col. 26, Line 55) disclose the step of oxidizing at least a portion of the first semiconductor layer comprises plasma oxidation at a temperature of about 150-450°C. However, given the substantial Hart et al., in view of Miyasaka et al, it would have been obvious to one with ordinary skill in the art at the time of the invention

to judiciously adjust and control the temperature of the oxidation process through routine experimentation and optimization to achieve optimum benefits (see MPEP 2144.05) and it would not yield any unexpected results.

9. Claim 108 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hart et al., (US 5,970,372) in view of McCollum et al.,(US 5,763,299) and further in view of Miyasaka (US 6,444,507).

Hart et al., disclose all claimed subject matter, but fails to expressly disclose the temperature of the oxidation process.

Miyasaka et al, in related text, (Col. 25, Line 63-Col. 26, Line 55) disclose the step of oxidizing at least a portion of the first semiconductor layer comprises plasma oxidation at a temperature of about 150-450°C. However, given the substantial Hart et al., in view of Miyasaka et al, it would have been obvious to one with ordinary skill in the art at the time of the invention to judiciously adjust and control the temperature of the oxidation process through routine experimentation and optimization to achieve optimum benefits (see MPEP 2144.05) and it would not yield any unexpected results.

10. Claim 108 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hart et al., (US 5,970,372) in view of McCollum et al.,(US 5,763,299) and further in view of Miyasaka (US 6,444,507).

Hart et al., disclose all claimed subject matter, but fails to expressly disclose the temperature of the oxidation process.

Miyasaka et al, in related text, (Col. 25, Line 63-Col. 26, Line 55) disclose the step of oxidizing at least a portion of the first semiconductor layer comprises plasma oxidation at a temperature of about 150-450°C. However, given the substantial Hart et al., in view of Miyasaka et al, it would have been obvious to one with ordinary skill in the art at the time of the invention to judiciously adjust and control the temperature of the oxidation process through routine experimentation and optimization to achieve optimum benefits (see MPEP 2144.05) and it would not yield any unexpected results.

Response to Arguments

11. Applicant's arguments with respect to claims 95-100 and 107-115 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (703) 305-0391. The examiner can normally be reached on Monday-Friday from 8:OOam to 5:OOpm.

If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms., can be reached on (703) 308-4910.

DV

David Vu.

David Nelms
Supervisory Patent Examiner
Technology Center 2800